CLAIMS

What is claimed is:

1. An interface transmitter coupled among a plurality of network elements of at least one network, wherein a plurality of data frames of a first type are received from at least one processor and stored in at least one random access memory (RAM), wherein data is read from the at least one RAM to at least one data serializer in response to a plurality of signals received from the at least one processor and over at least one backplane network, wherein a plurality of data frames of a second type corresponding to the plurality of data frames of a first type are generated and serially transferred among the plurality of network elements using the at least one backplane network.

2. The interface transmitter of claim 1, wherein the at least one data frame of a second type comprises switching event information of the plurality of network elements.

3. The interface transmitter of claim 1, wherein the at least one backplane network is further coupled to transfer the at least one data frame of a second type among at least one receiver and the at least one processor, wherein compare operations are performed among prespecified data frames of a second type at prespecified intervals, wherein at least one interrupt signal is generated in response to data changes determined by the compare operations, wherein protection switching is controlled in the at least one network by the at least one processor in response to the at least one interrupt signal.

4. The interface transmitter of claim 3, wherein generating at least one interrupt signal comprises generating at least one unit interrupt signal in

response to the data changes, generating at least one memory map in response to the at least one unit interrupt signal, and generating at least one massive interrupt signal in response to the at least one unit interrupt signal.

5. The interface transmitter of claim 1, wherein protection switching is controlled in the plurality of network elements by the at least one processor in response to the switching event information, wherein the at least one processor navigates among a plurality of memory locations using a plurality of memory maps in response to at least one interrupt signal, reads data from the plurality of memory locations relating to the switching event information, and evaluates the switching event information.

6. The interface transmitter of claim 1, wherein the at least one backplane network comprises a 16-channel bus.

7. The interface transmitter of claim 1, wherein the plurality of data frames of a first format correspond to a plurality of input channels among the plurality of network elements.

8. The interface transmitter of claim 1, wherein the at least one RAM comprises a plurality of memory areas distributed among the plurality of network elements.

9. The interface transmitter of claim 1, wherein the at least one RAM comprises at least one dual port RAM.

10. The interface transmitter of claim 1, wherein the storing comprises multiplexing the plurality of data frames of a first type into at least one field-programmable gate array (FPGA).

11. The interface transmitter of claim 1, wherein the at least one data frame of a second type comprises approximately 67.5 bytes comprising

status bytes and Synchronous Optical Network (SONET) bytes including K1, K2, E1, and F1 bytes transferred as a serial bit stream at a rate of approximately 4.32 megahertz.

12. The interface transmitter of claim 1, wherein the at least one processor includes a plurality of processors distributed among the plurality of network elements.